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(57) Abstract :

The high-speed neuron implementation system comprises an artificial neuronal encoder to encode an input data into a neuronal code; a pre-processing unit to pre-process a code deviation data of the neuronal code; a Vedic multiplier to determine a first product and a second product of a component of a code deviation accumulation data, a masking factor, and a component of a code deviation data; a first Vedic adder to calculate a first sum of first products; a second Vedic adder to calculate second product of an entry of a code covariance matrix, a masking factor, and a component of a code deviation data; and a central processing unit to determine a second sum of second products obtained by the second Vedic adder, and to use the second sum and first sum determined by the central processing unit to calculate representation of empirical probability distribution of a component of labelled data.

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